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(54) Thin panel display

(57) A multilayer display apparatus comprises a transparent outer layer (12), a first (16) and a second (18) electrode beneath said outer layer, each said electrode having portions transversely spaced from portions of the other said electrode (eg interdigitated), a layer (20) of electroluminescent material beneath said first and second electrodes, and one or more third electrodes (24) beneath said luminescent layer, each third electrode extending transversely over a display area of said luminescent layer defining an individual display element, whereby energization of a third electrode simultaneously with energization of said first and second electrodes produces luminescence of the corresponding element, visible through the gaps between the first and second electrodes.

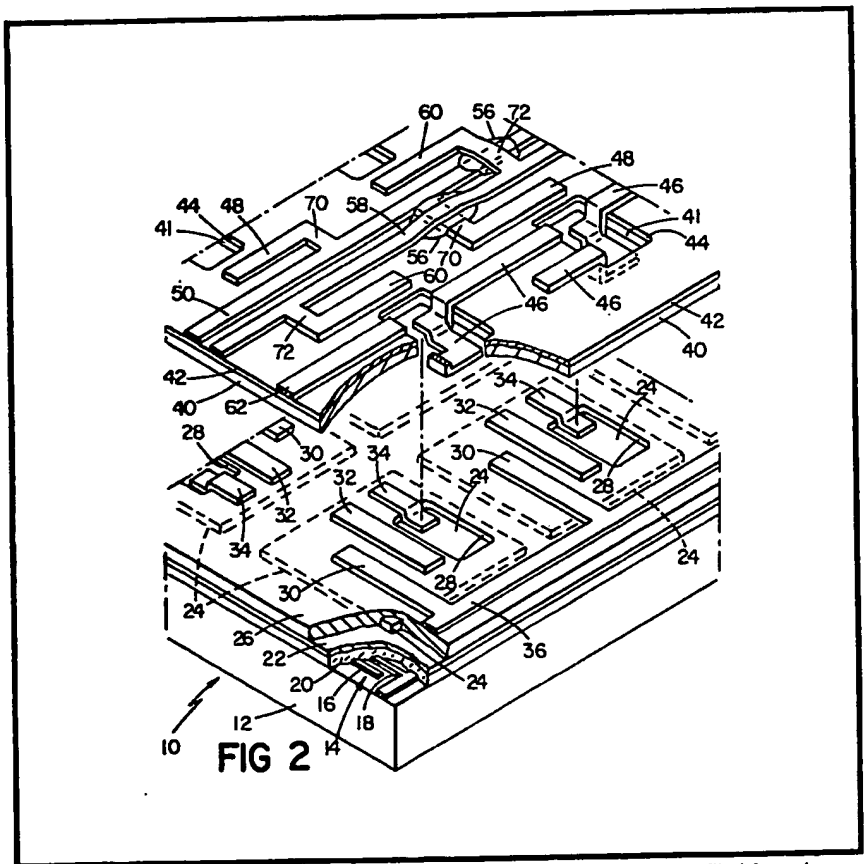


FIG 2

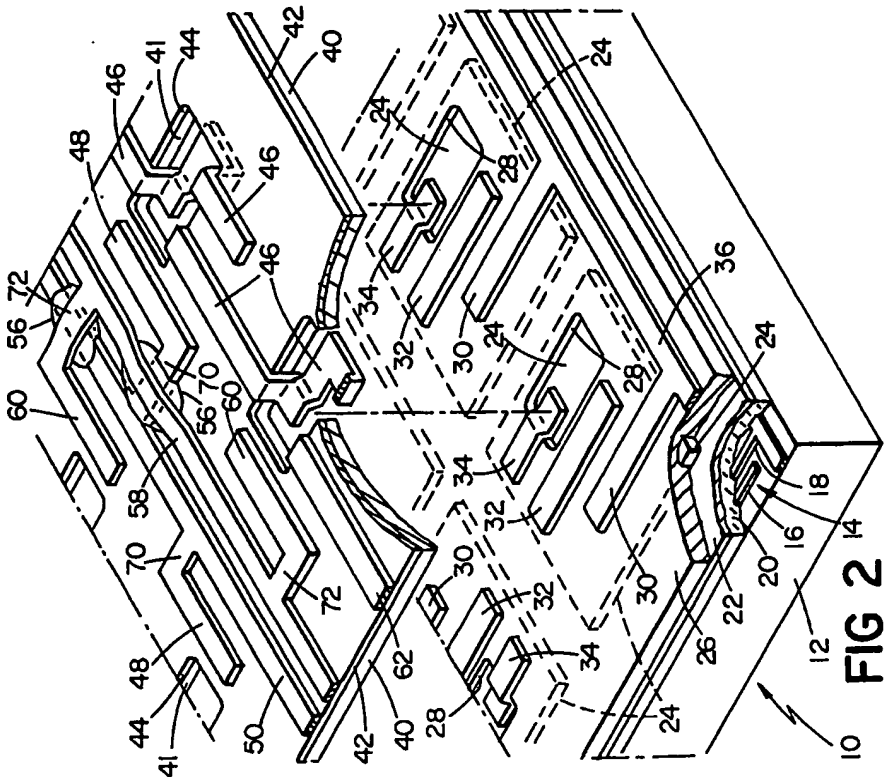


FIG 2

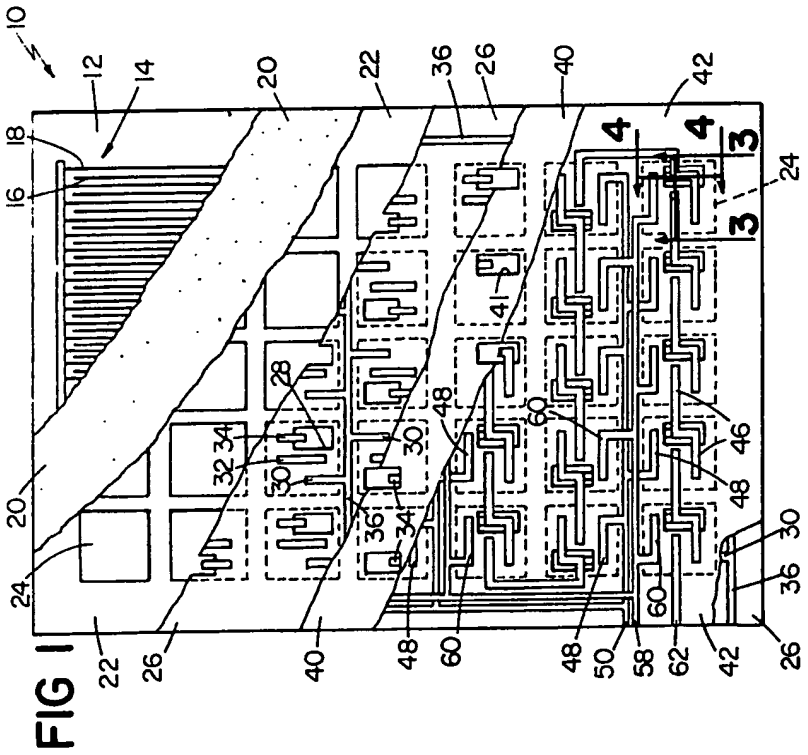


FIG 1

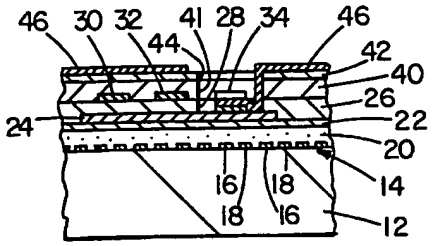


FIG 3

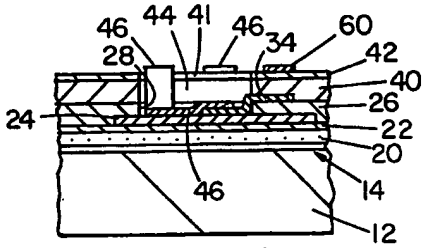


FIG 4

FIG 5

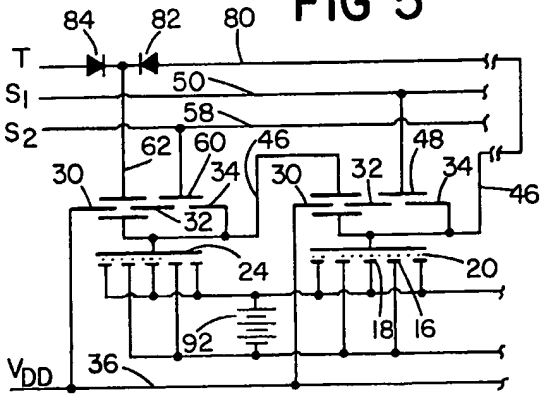
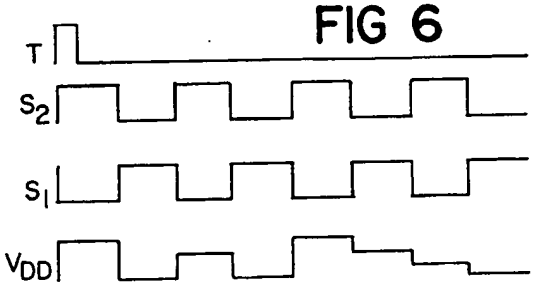


FIG 6



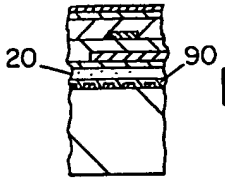


FIG 7

SPECIFICATION

Thin panel display

In many display applications, including television and alphanumeric displays, it is desirable to have mounted on a thin panel a matrix of discrete, closely-spaced radiation-emitting elements which can be individually controlled over a wide brightness range.

Commercial television and some alphanumeric displays presently rely on the bulky cathode ray tube to control luminescent elements on a display screen. Good brightness range is achieved, and few connection leads are required, but the size of the tube is a drawback for many applications.

Various thin panel display devices have been proposed, but these have generally relied on row and column addressing and thus have required as many as 1040 external connections for controlling a 520 by 520 element display. For example, Luo et al. U.S. Patent No. 4,042,854 shows an AC-driven electroluminescent display with leads for each row and column and a pair of thin-film transistors and a capacitor at each display element.

When electroluminescent devices are used as the radiation-emitting elements, increased brightness is generally desired, and it is also desirable to produce satisfactorily bright luminescence with the same level DC voltages as are commonly used in CMOS logic devices (approximately 15 volts DC), thereby eliminating the additional cost of converting logic output signals to higher voltages for producing luminescence. A difficulty with conventional electroluminescent devices is that, when a sandwich construction (two area electrodes on either side of a luminescent layer) is used, the transparent electrode placed between the transparent substrate and the luminescent film, by virtue of its thinness and high resistance, contributes to detrimental capacitance effects which limit operating speed and frequency. It would thus be desirable to have an electroluminescent display element with sufficiently thick electrodes all on one side of the luminescent layer.

Several references have shown electroluminescent devices that employ transversely-spaced electrodes on one side of a luminescent layer. Kanie U.S. Patent No. 3,519,871 and Mash U.S. Patent No. 2,928,974 show the electrodes positioned opposite the viewing side of the luminescent layer. Kanie suggests direct-current operation and shows a vacuum-deposited luminescent layer. Robinson U.S. Patent No. 3,312,825 shows AC-sensitive, semiconductive luminescent material filling wide gaps between transversely spaced electrodes. Mager et al. U.S. Patent No. 2,628,974 shows an AC-sensitive layer composed of a dielectric base material filled with small phosphor particles covering the electrodes. Vecht U.S. Patent No. 3,731,353 shows a DC-sensitive device that produces luminescence only along narrow zones.

Vlasenko et al. U.S. Patent No. 3,889,016 shows a method for producing a DC-sensitive electroluminescent film by vacuum deposition.

In our co-pending Application No. 7940501 there is described and claimed an invention which, in one aspect, features adding a plurality of thin-film transistor circuits to a multilayer display apparatus having a transparent outer layer and a plurality of discrete radiation-emitting elements beneath the outer layer, the circuits being located beneath the radiation-emitting elements, with one circuit being adjacent to and associated with at least one of the elements, and the circuitry including switching means for supplying a common brightness control signal to the control electrode of the associated radiation-emitting element when an arming signal from a preceding circuit and a common timing signal are sensed, means for maintaining the switching means in a conductive state for a time sufficiently long enough to energize the radiation-emitting element, and means for supplying an arming signal to the next successive circuit; leads for supplying the common timing and brightness signals are connected to the circuits and selection means are provided to make adjacent circuits sensitive to different states of said timing signal. State changes in the timing signal cause the transistor circuits to switch the brightness control signal from one radiation-emitting element to another in a continuous scan across the whole display apparatus. In this aspect, the invention provides a means of controlling the brightness of a large matrix of display elements with very few external leads (e.g., four in the preferred embodiment), thereby greatly simplifying the external circuitry required for controlling the display panel. Furthermore, the panel can be manufactured using known thin-film deposition processes in the large dimensions required for television, billboards and the like as well as in smaller dimensions for alphanumeric displays, while also maintaining the desired thinness. In preferred embodiments, two timing signals 180° out of phase with each other are supplied on two separate leads, and the leads are connected alternately to successive circuits to assure that adjacent circuits are not simultaneously responsive to the timing signals; a gate connected to the control electrode serves to latch the switching means on after the arming signal from the preceding circuit has been removed; a lead extending from the same gate and thus also connected to the control electrode is connected to a gate of the succeeding circuit and thereby provides the arming signal; the switching means includes a first drain connected to the common brightness signal, a second intermediate drain, a source connected to the control electrode, two

gates controlling the connection between the first and second drains, one gate connected to the arming lead from the preceding transistor and the other to the control electrode for latching, and a single timing gate controlling the connection between the second drain and the source, the timing gate being alternately connected in successive circuits to one or the other of two timing signal leads; and the radiation element is an electroluminescent element with an area electrode as the control electrode.

In one aspect, the present invention features an electrode grid beneath the outer transparent layer of a display device and a continuous, generally uniform thickness film of electroluminescent material vacuum deposited beneath the electrode grid. The electrode grid provides transparency by virtue of the spacing between adjacent electrodes but is much more conductive than transparent electrodes, thereby reducing capacitive effects and extending the maximum frequency of operation. In the most preferred embodiment, the electroluminescent film contacts the grid, is suitably doped with copper and manganese so as to be sensitive to direct current and is subjected to between 15 and 25 volts D.C. and the grid consists of two electrodes having intermeshed narrow portion between 0.5 and 1.5 mils wide and spaced from each other between 0.5 and 5 mils. In another preferred embodiment, a current-limiting layer (e.g., Y_2O_3 between 800 and 3000 angstroms thick) is interposed between the grid and electroluminescent material which lacks the copper doping and is operated in a field-induced, AC-voltage luminescence mode.

In another aspect, the present invention features adding a third area electrode beneath the luminescent layer and grid electrodes. Voltage applied to the third electrode modulates the brightness of the luminescence viewed through the transparent substrate. In the most preferred embodiment, an insulating layer is placed between the luminescent layer and the third electrode, the two other electrodes have portions forming an electrode grid, the grid contacts the electroluminescent material to allow current flow through the material, and D.C. voltages are applied to the grid and third electrodes. The D.C. voltage at the third electrode causes "holes" (positive carriers) in the luminescent material to drift toward the electrode grid, thereby creating more recombination centers for luminescence near the grid, whereby the brightness of the luminescence may be controlled by the third electrode potential and greater brightness may be achieved at the low D.C. voltages customarily used with CMOS devices (e.g., 16 volts). In another preferred embodiment, a current-limiting insulating layer separates the electrode grid from the luminescent material, and an AC voltage is applied either to the third electrode or the grid, and a DC voltage is applied to the other; the luminescent material is thus made responsive only to the electric field, and the combination of AC and DC voltages enhance brightness.

In still another aspect, the invention features aligning dipoles within the crystal structure of a layer of electroluminescent material by depositing the material in the presence of an electric field. In preferred embodiments, the electric field is generated by a DC voltage applied across an electrode grid on which the luminescent material is deposited. The aligned-dipole crystal structure exhibits enhanced brightness.

We turn now to the structure and operation of preferred embodiments of the invention, after first briefly describing the drawings.

Figure 1 is an overall plan view of the most preferred embodiment, with portions of various layers cut away.

Figure 2 is a perspective view of one corner of said embodiment, with portions cut away and with the semiconductor, insulator, and gate layers shown exploded above underlying layers.

Figure 3 is a cross-sectional view at 3–3 of Fig. 1.

Figure 4 is a cross-sectional view at 4–4 of Fig. 1.

Figure 5 is a schematic view showing electrical operation of said embodiment.

Figure 6 shows input waveforms.

Figure 7 is a partal cross-sectional view of a second preferred embodiment at a location equivalent to 3–3 of Fig. 1, showing a current-limiting layer between the electrode grid and the luminescent layer.

Referring to Fig. 1, there is shown electroluminescent display panel 10. A five by seven matrix of discrete luminescent elements, which when selectively illuminated form alphanumeric characters, is formed by deposition of various layers on glass substrate 12 (1/16 inch thick), through which the luminescence is observed.

Electrode grid 14 is formed on substrate 12 by vacuum depositing a thin (1000 angstroms) film of aluminum on the upper surface of the substrate and then vaporizing a 1 mil wide convoluted gap using a laser beam focused to that width. This leaves two electrical pathways consisting of 1 mil wide electrode fingers 16, 18 spaced 1 mil part. Electroluminescent layer 20 of zinc sulfide activated with maganese and copper is vacuum deposited without masking over electrode grid 14 to a thickness of 2 microns, which provides sufficient capacitance. A 25 V.D.C. potential is applied across grid 14 during deposition of layer 20 so as to align dipoles in the zinc sulfide crystalline structure. A forming current is applied to the electroluminescent material after deposition to move copper ions to the grounded electrode of grid 14. The copper

ions form a thin p-type region at the grounded electrode. Insulator layer 22 of Al_2O_3 is vacuum deposited over layer 20 to a thickness of 3000 angstroms, also without masking. At that thickness the Al_2O_3 is transparent. (All vacuum depositing is performed at or below 1×10^{-5} torr.)

Additional layers above layer 22 are deposited using one of six deposition masks. Rear electrodes 24, consisting of thirty-five discrete aluminum squares (30 mils square; spaced 10 mils apart) arranged in a five by seven matrix, are vacuum deposited to a thickness of 2500 angstroms using mask #1, which has square holes. Second insulator layer 26 of Al_2O_3 is deposited to a 1000 angstrom thickness over rear electrodes 24, using mask #2 to form rectangular holes 28 with rounded corners.

Above insulator layer 26, a matrix of thin-film switching transistors is deposited. A pattern of three gold electrodes—drains 30, intermediate drains 32, and sources 34—are deposited aligned with each rear electrode 24 to a 1000 angstrom thickness, using mask #3. Drains 30 are all interconnected in one electrical circuit by 1000 micron wide drain lead 36. Each of electrodes 30, 32, 34 is 300 microns wide and spaced 50 microns from adjacent electrodes. Gold is used for electrodes 30, 32, 34 to assure good ohmic contact with semiconductor layer 40. Sources 34 extend over the edge of holes 28 and contact rear electrodes 24 (Fig. 2). To achieve deposition of the gold on the vertical face (Fig. 2) of hole 28, the deposition is performed at oblique angles to layer 26. Semiconductor layer 40 of CdS is deposited over electrodes 30, 32, 34 to a thickness of 3000 angstroms, using mask #2. A third insulator layer 42 of Al_2O_3 is deposited over the semiconductor layer, to a thickness of 600 angstroms, also using mask #2. Holes 41, 44 produced in layers 40, 42, respectively, are aligned with hole 28 in layer 26.

Above the insulator and semiconductor layers, a pattern of generally horizontal gate electrodes and associated leads are deposited in two stages. First, timing signal lead 50, branch leads 70, gates 48 and interelement gates 46, all aluminum, are deposited to a thickness of 2000 angstroms, using mask #4. Interelement gates 46 extend downward into aligned holes 28, 41, 44 to contact sources 34 and rear electrodes 24, and deposition is conducted at an oblique angle to layer 42 to assure adequate deposition of gates 46 on vertical faces of holes 28, 41, 44. To insulate at crossover points, insulator spots 56 of Al_2O_3 (1000 angstroms thick) are deposited over selected areas of lead 50 and gates 48 (Fig. 2), using mask #5. Finally, second timing signal lead 58, branch leads 72, and gates 60 are deposited, to a thickness of 2000 angstroms, using mask #6. Timing signal leads 50, 58 are 1000 microns wide; gates 46, 48, 60 are 300 microns wide. Epoxy potting (not shown) is applied over the entire upper surface for sealing and insulating. A separate lead 62, carrying a start signal, serves as a gate for the lower left-hand element (Fig. 1). Six leads extend to the lower left-hand edge of panel 10 (Fig. 1) for making external connections: timing signal leads 50, 58; start signal leads 62; drain lead 36; and leads (not shown) connecting electrode fingers 18, 20.

After deposition of each of the various layers, monolayers (layers only one molecule thick) of absorbed gases are cleaned off by glow discharge bombardment before deposition of succeeding layers.

Referring to Fig. 7, there is shown a second embodiment in which insulator layer 90 of Y_2O_3 (1300 angstroms thick) is deposited over electrodes 16, 18 to limit current flowing through the luminescent layer. In that embodiment, a phosphor layer sensitive to alternating current is used, for example, ZnS:Mn without copper doping.

Display panel 10 consists of 35 individual luminescent elements. Each element is energized by a low D.C. voltage (between 5 and 10 V.D.C.) applied across electrodes 16, 18 (Fig. 5) and by a second D.C. voltage (4–15 V.D.C.) applied to rear electrode 24. The voltage across electrodes 16, 18 is set low enough that it alone is insufficient to cause significant visible luminescence; rear electrode 24 must also be energized for significant luminescence to occur. One of electrodes 16, 18 is grounded. The positive voltage at electrode 24 causes "holes" (positive carriers) in the electroluminescent material to drift toward electrodes 16, 18, thereby providing more recombination centers in the grid region and thus more visible luminescence. Insulator layer 22 isolates electrode 24 to provide field-effect operation.

The voltage across electrodes 16, 18 is supplied by voltage source 92 (Fig. 5) on leads not shown in the figures. The voltage applied at each of the thirty-five electrodes 24 corresponds to the instantaneous value of V_{DD} (Figs. 5 and 6) during the interval in which a particular electrode 24 is energized. The matrix of interconnected thin film transistors sequentially energizes individual electrodes 24 by switching V_{DD} onto the electrodes in a periodic scan.

Start signal T (A short-duration 4 V.D.C. pulse) on leads 62 begins the scan by putting into saturation the transistor formed by gate 62, drain 30 and intermediate drain 32 in the first matrix element in the lower left-hand corner of the panel (Figs. 1 and 2), in effect closing a first switch across drains 30, 32 (Fig. 6). Coincident with this action, signal S_2 (4 V.D.C. in high state; 0.0 V.D.C. in low) on lead 58 drives into saturation the transistor defined by gate 60, intermediate drain 32,

the source 34 in effect closing a second switch (Fig. 5). With both first and second switches simultaneously closed. electrode 24 is energized by signal V_{DD} and luminescence occurs at the first element in proportion to the voltage level of V_{DD}. The V_{DD} signal also appears on interelement gate 46, which is common with source 34, and thus serves as a latch to hold closed the first switch, between drains 30, 32, after start signal T disappears.

At the end of the first time interval, S_2 goes low (0.0 V.D.C), and S_1 goes high (4 V.D.C.) (Fig. 6). This has the effect of de-energizing the first electrode 24 (because the second switch is opened) and energizing the next downstream electrode 24. The V_{DD} voltage on interelement gate 46 has armed the next element by closing the first switch (one portion of the gate acting as an arming lead), and signal S_1 on lead 50 and gate 48 has closed the second switch. The first switch is then held closed by the latching effect of the second interelement gate 46.

Each element in the five by seven matrix is thus periodically energized by V_{DD}. Sufficient luminescence persistence is provided by the manganese activated zinc sulfide to allow a 1/75 second period between successive applications of V_{DD} to any one element. Return lead 80 connects the interelement gate 46 of the last element through diode 82 to start gate 62. Diode 84 works in conjunction with diode 82 to prevent start signal T from energizing return lead 80 and vice versa. Both diodes are mounted on the periphery of panel 10.

The minimum voltage level of signal V_{DD} is selected to be high enough to latch the first switch of each element while not also causing any visible luminescence, and the maximum voltage level of V_{DD} corresponds to maximum desired luminescence.

To prevent simultaneous energization of all elements, timing signals S_1 and S_2 have non-coincident edges, S_2 going low slightly before S_1 goes high and similarly for successive time periods. Inherent capacitance holds interelement gates 46 on a sufficient time for the successing element to latch on.

In the most preferred embodiment, luminescence is caused by current conduction through layer 20 between electrode 16, 18, the amount of current being modulated by the voltage V_{DD} applied to rear electrodes 24. In the second preferred embodiment shown in Fig. 7, luminescence is a function wholly of the field applied across grid electrodes 16, 18 and to rear electrode 24. Insulating layer 90 of Y_2O_3 prevents current flow across the grid. To operate the second embodiment, a low-level AC voltage is applied across grid electrodes 16, 18, and a DC voltage is used on rear electrode 24 to modulate the luminescence. The combination of AC and DC voltage signals gives improved brightness. See the article by W.A. Thornton entitled "AC–DC Electroluminescence" published in Physical Review, Vol. 113, No. 5, on March 1, 1959, wherein an AC-modulated DC voltage was applied in a two-electrode structure across a luminescent layer sandwiched between electrodes.

Application of the 25 V.D.C. potential across grid electrodes 16, 18 during deposition of the luminescent layer influences the crystal structure of the ZnS during nucleation, agglomeration, and subsequent growth stages sufficiently to better expose luminescent portions of the ZnS and thereby increase brightness.

CLAIMS

1. A multilayer display apparatus, comprising: a transparent outer layer, a first and a second electrode beneath said outer layer, each said electrode having portions transversely spaced from portions of the other said electrode, a layer of electroluminescent material beneath said first and second electrodes, and a third electrode beneath said luminescent layer, said third electrode extending transversely over a display area of said luminescent layer and said display area defining an individual display element of said display apparatus, whereby energization of said first and second electrodes produces luminescence at said area of said luminescent layer.

2. A display apparatus as claimed in claim 1 further comprising an insulating layer between said luminescent layer and said third electrode, whereby current is substantially prevented from flowing at said third electrode and voltage applied to said third electrode may create a field in said electroluminescent material to move charge carriers normal to said electrode such that the brightness of luminescence visible through said transparent outer layer is varied.

3. A display apparatus as claimed in claim 1 further comprising a current-limiting layer between said electroluminescent material and said first and second electrodes, whereby current is substantially prevented from flowing between said first and second electrodes and luminescence is influenced by the electric field generated between said electrodes.

4. A display apparatus as claimed in claim 1 wherein said apparatus further comprises an insulating layer beneath said luminescent layer and a plurality of third electrodes in addition to said first mentioned third electrode beneath said insulating layer, each said third electrode extending transversely over a display area of said luminescent layer and said display areas defining a matrix of individual display elements and said first and second electrode each have a plurality of portions transversely intermeshed with and spaced from corresponding portions of the other said electrode to form an electrode grid extending across an

area encompassing a plurality of said display areas, whereby energization of said grid for said plurality of display areas is accomplished by application of a potential to said first and second electrodes and the luminescence at individual display areas is controlled by the potential applied to said third electrodes.

5. A display apparatus as claimed in any one of the preceding claims, wherein said first and second electrodes are a plurality of electrodes beneath said outer layer, said layer of electroluminescent material beneath said electrodes, the crystal structure of said material having aligned dipoles, whereby application of an electric field across said luminescent material with aligned dipoles produces luminescence of increased brightness over that of the same luminescent material without aligned dipoles.

6. A display apparatus as claimed in claim 5 wherein said plurality of electrodes comprise a first and a second electrode, each said electrode having portions transversely intermeshed with and spaced from corresponding portions of the other said electrode to form an electrode grid, whereby application of an electric potential to said grid during deposition of the electroluminescent material causes the desired alignment of dipoles in the crystal structure of said material.

7. A method of producing a display apparatus as claimed in claim 5, comprising the steps of: applying an electric field in the region adjacent a deposition surface of said substrate and vacuum depositing said electroluminescent material on said substrate in the presence of said electric field, thereby causing the resulting crystal structure of said material deposited on said substrate to have aligned dipoles.

8. A method according to claim 7 wherein the direction of said electric field is transverse to the normal of said deposition surface of said substrate.

9. A method according to claim 8 wherein said transverse electric field is generated by applying a D.C. voltage between transversely spaced electrodes on said substrate.

10. A display apparatus as claimed in claim 1, wherein the transparent outer layer is a dielectric layer, an electrode grid is supported on the inside surface of said outer layer, said grid including said first and second electrodes with transversely intermeshing portions, the width of said intermeshing portions being equal to or less than the width of the gaps between them, and the layer of electroluminescent material is a continuous, generally uniformly-thick film of vacuum-deposited semiconductive material, whereby application of a potential to said electrodes produces luminescence in said film and whereby the separation between said electrodes is sufficient to allow substantial light transmission between electrodes and through said outer layer.

11. An apparatus as claimed in claim 10 further comprising a dielectric film between said grid and semiconductive electroluminescent material, whereby said dielectric film allows an AC voltage applied across said grid to produce area luminescence.

12. An apparatus as claimed in claim 10 wherein said film of semiconductive electroluminescent material is doped so as to be sensitive to direct-current and said film contacts said grid, whereby area luminescence is produced by application of a DC voltage.

13. An apparatus as claimed in claim 10 wherein said film has greater than twice the thickness of said electrodes, whereby luminescence occurs in the gaps between said electrodes and in regions beneath said electrodes.

14. An apparatus as claimed in claim 10 wherein said grid electrodes have a transverse width of between 0.5 and 1.5 mils and a transverse spacing of between 0.5 and 5 mils.

15. A method of producing a display apparatus as claimed in claim 1, comprising the steps of: vacuum depositing a continuous layer of conductive electrode material; selectively removing a convoluted region of said electrode material to leave an electrode grid composed of two electrodes with transversely intermeshing portions, and vacuum depositing a continuous layer of semiconductive electroluminescent material over the grid.

16. A method according to claim 15 further comprising the steps of vacuum depositing a continuous layer of dielectric material over the grid before vacuum depositing the electroluminescent material.

17. A multilayer display apparatus as claimed in claim 1 and substantially as hereinbefore described with reference to any one of Figs. 1 to 6 of the accompanying drawings.

18. A multilayer display apparatus as claimed in claim 1 and substantially as hereinbefore described with reference to Fig. 7 of the accompanying drawings.

19. A method of producing a display apparatus, according to claim 7 or 15 and substantially as hereinbefore described with reference to any one of the accompanying drawings.

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